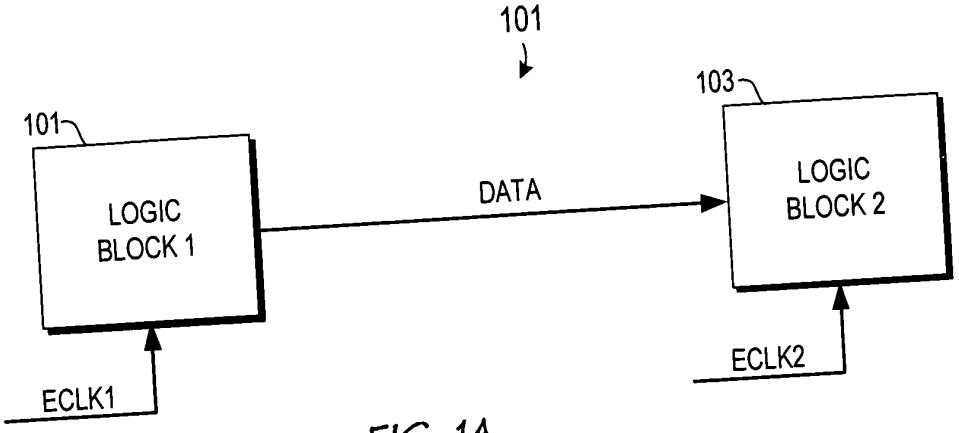
101
101
LOGIC
BLOCK 1
DATA
103
LOGIC
BLOCK 2
ECLK1
ECLK2

FIG. 1A

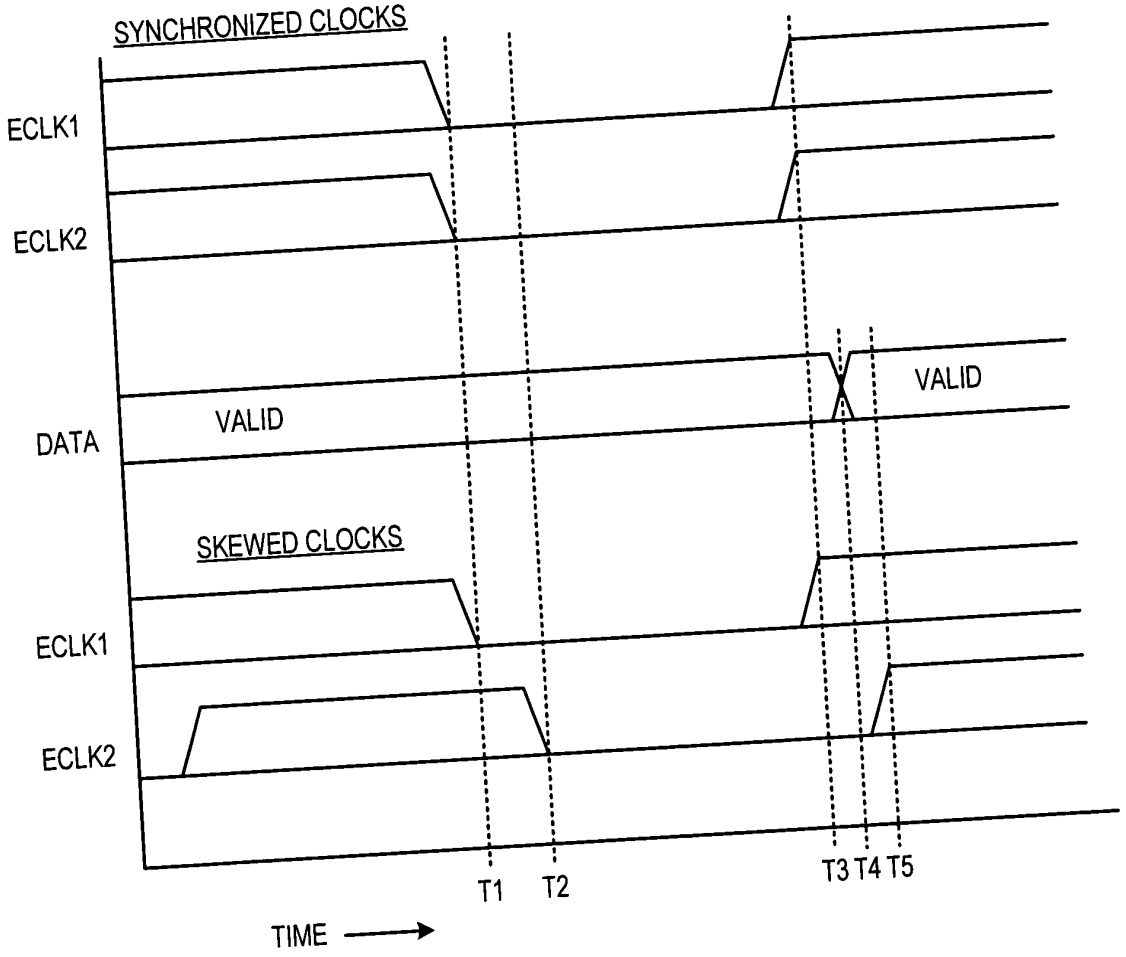
SYNCHRONIZED CLOCKS
ECLK1
ECLK2
VALID
VALID
DATA
SKEWED CLOCKS
ECLK1
ECLK2
T1
T2
T3
T4
T5
TIME

FIG. 1B

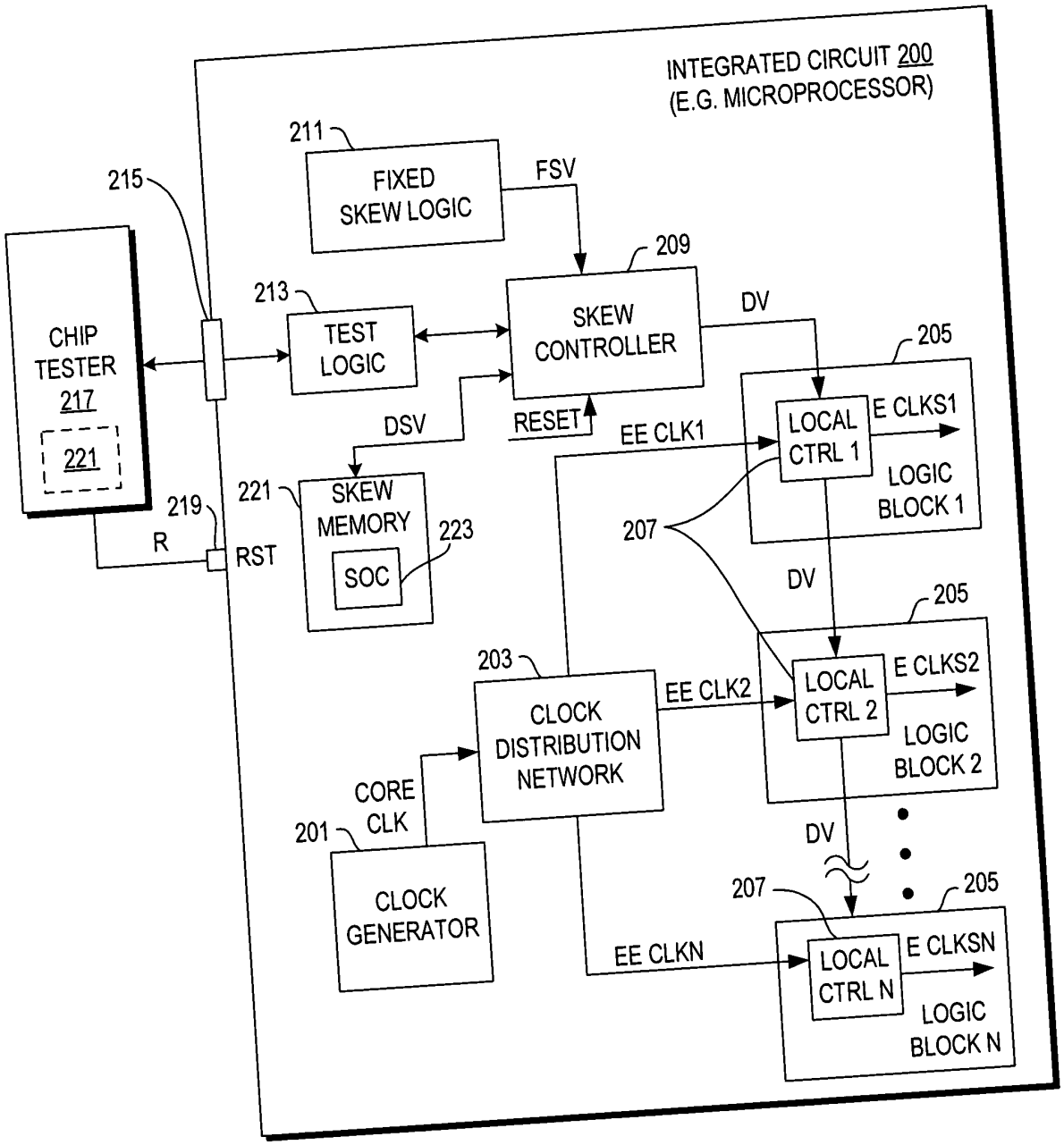
INTEGRATED CIRCUIT 200
(E.G. MICROPROCESSOR)
211
FIXED SKEW LOGIC
FSV
215
209
213
TEST LOGIC
SKEW CONTROLLER
DV
205
CHIP TESTER 217
221
DSV
RESET
EE CLK1
LOCAL CTRL 1
E CLKS1
LOGIC BLOCK 1
219
R
RST
221
SKEW MEMORY
223
SOC
207
DV
205
203
CLOCK DISTRIBUTION NETWORK
EE CLK2
LOCAL CTRL 2
E CLKS2
LOGIC BLOCK 2
CORE CLK
201
CLOCK GENERATOR
DV
207
205
EE CLKN
LOCAL CTRL N
E CLKSN
LOGIC BLOCK N

FIG. 2

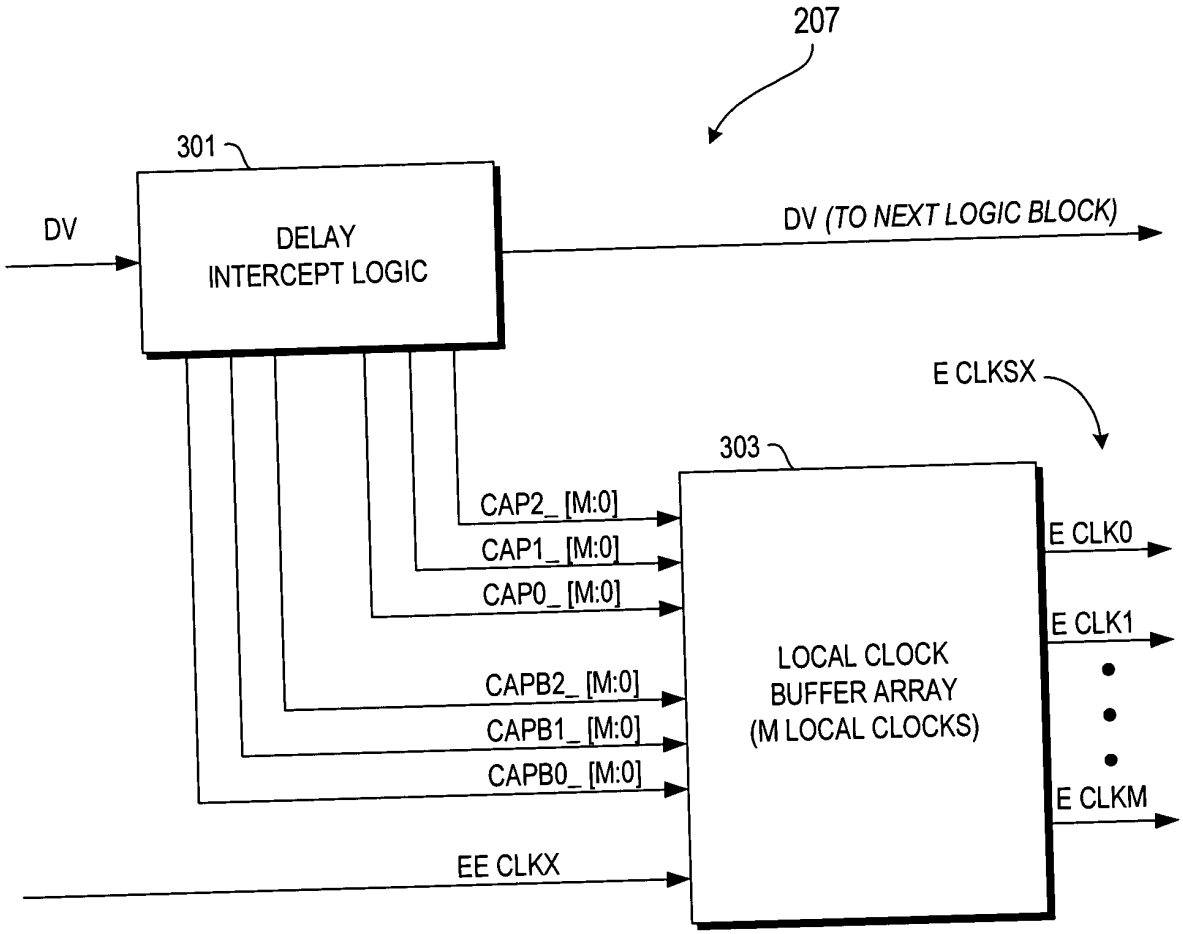
207
301
DV
DELAY
INTERCEPT LOGIC
DV (TO NEXT LOGIC BLOCK)
E CLKSX
303
CAP2_ [M:0]
CAP1_ [M:0]
CAP0_ [M:0]
CAPB2_ [M:0]
CAPB1_ [M:0]
CAPB0_ [M:0]
EE CLKX
LOCAL CLOCK
BUFFER ARRAY
(M LOCAL CLOCKS)
E CLK0
E CLK1
E CLKM

FIG. 3

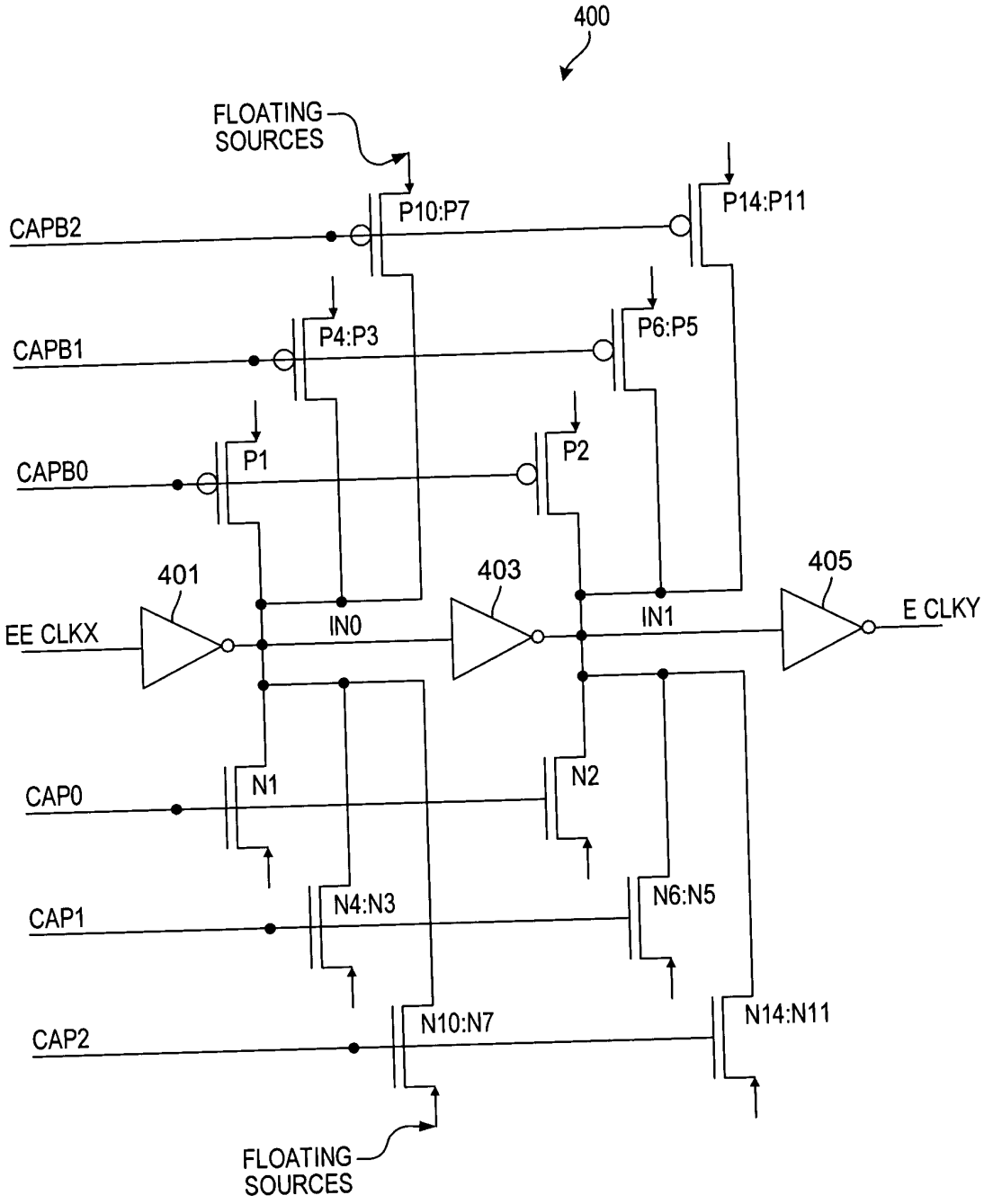
400
FLOATING SOURCES
CAPB2
P10:P7
P14:P11
CAPB1
P4:P3
P6:P5
CAPB0
P1
P2
401
403
405
EE CLKX
IN0
IN1
E CLKY
CAP0
N1
N2
CAP1
N4:N3
N6:N5
CAP2
N10:N7
N14:N11
FLOATING SOURCES

FIG. 4